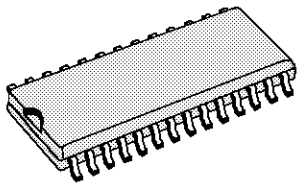
SGS-THOMSON MICROELECTRONICS

STV0180

HIGH SPEED 8-BIT ADC

ADVANCE DATA

- 8 BIT RESOLUTION
- SAMPLING RATE UP TO 30MHz
- BINARY OR 2's COMPLEMENT TRISTATE OUTPUTS
- OVERFLOW/UNDERFLOW TRISTATE OUTPUTS
- TTL-COMPATIBLE DIGITAL OUTPUTS
- LOW-LEVEL AC CLOCK INPUT SIGNAL ALLOWED
- INTERNAL VOLTAGE REFERENCE GENERATOR
- NO SAMPLE AND HOLD CIRCUIT REQUIRED
- SO28 PLASTIC PACKAGE



SO28
(Plastic Package)

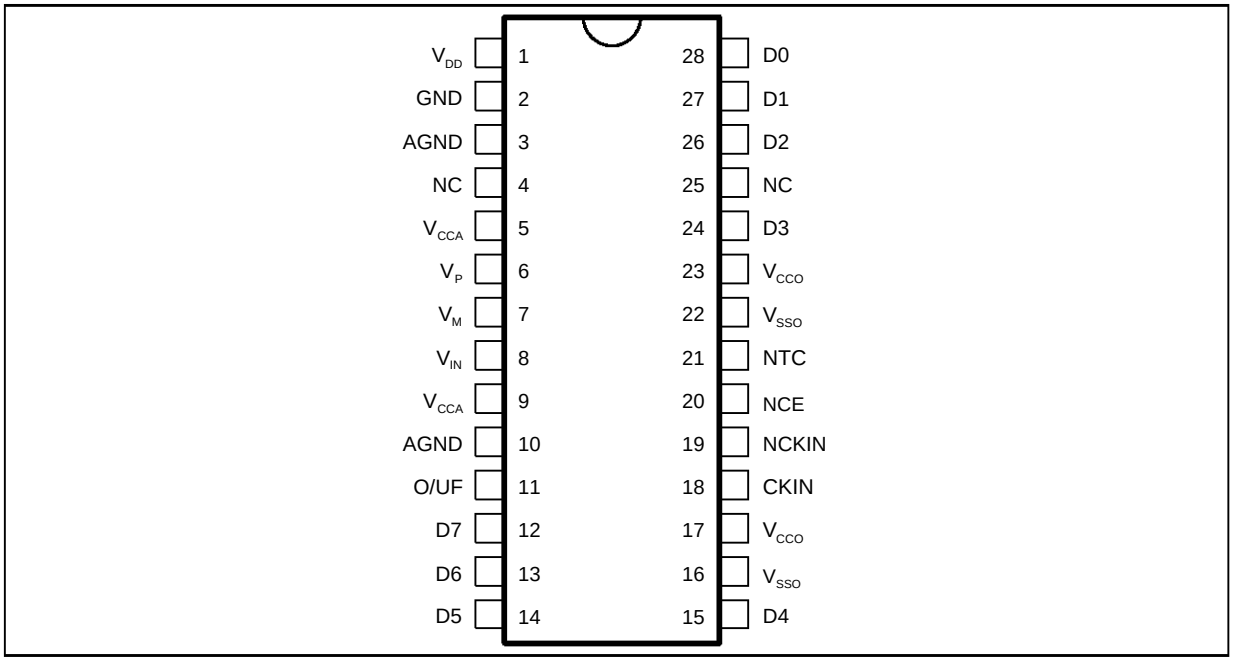
ORDER CODE : STV0180

DESCRIPTION

The STV0180 is an 8-bit Analog-to-Digital Converter specially designed for use in video and others high quality applications.

The technology used to achieve the needed quality is a BiCMOS 1.2µm process.

PIN CONNECTIONS



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PIN DESCRIPTION

Pin N°	Name	Description
1	V_{DD}	Positive Supply Voltage for Digital Part (5V)
2	GND	Digital Ground
3	AGND	Analog Ground
4	NC	Not Connected
5	V_{CCA}	Positive Supply Voltage for Analog Part (5V)
6	V_P	Top Reference Voltage Decoupling
7	V_M	Bottom Reference Voltage Decoupling
8	V_{IN}	Analog Voltage Input
9	V_{CCA}	Positive Supply Voltage for Analog Part
10	AGND	Analog Ground
11	O/UF	Overflow/Underflow Data Output
12	D7	Data Output Bit 7 (MSB)
13	D6	Data Output Bit 6
14	D5	Data Output Bit 5
15	D4	Data Output Bit 4
16	V_{SSO}	Ground for Output Stages
17	V_{CCO}	Positive Supply Voltage for Output Stages (5V)
18	CKIN	Clock Input
19	NCKIN	Negative Clock Input
20	NCE	Chip Enable Input (TTL Level, Active Low)
21	NTC	Input for 2's Complement Output (TTL Level, Active Low)
22	V_{SSO}	Ground for Digital Outputs
23	V_{CCO}	Positive Supply Voltage for Output Stages (5V)
24	D3	Data Output Bit 3
25	NC	Not Connected
26	D2	Data Output Bit 2
27	D1	Data Output Bit 1
28	D0	Data Output Bit 0 (LSB)

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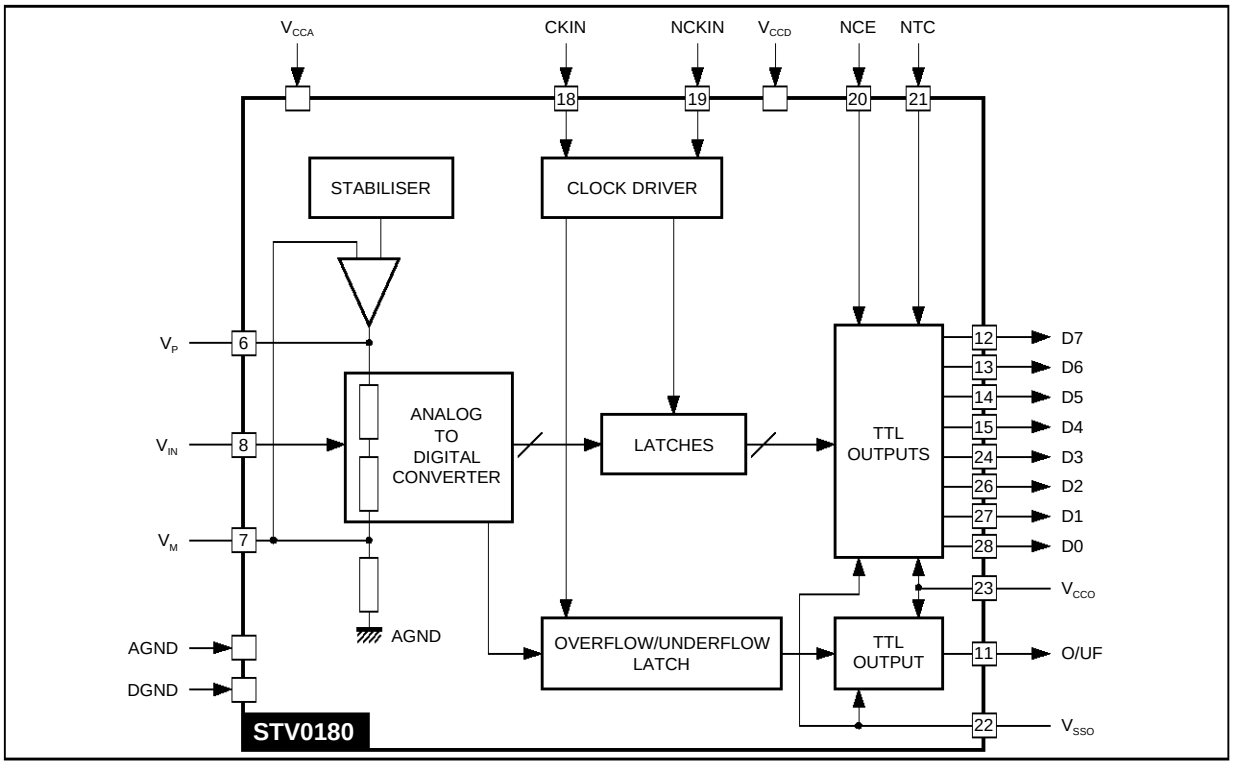
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{CCA}	Analog Supply Voltage		-0.3	7	V
V_{DD}	Digital Supply Voltage		-0.3	7	V
V_{CCO}	Output Stages Voltage Supply		-0.3	7	V
V_{CCA} - V_{CCD}	Supply Voltage Differences		-1	1	V
V_{CCA} - V_{DD}	Supply Voltage Differences		-1	1	V
V_{CCO} - V_{DD}	Supply Voltage Differences		-3	1	V
V_{VI}	Input Voltage	Referenced to AGND	-0.3	7	V
I_O	Output current		-10	10	mA
T_{amb}	Operating Ambiant Temperature		0	70	°C

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ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{CCA} = V_{CCO} = 4.75$ to $5.25V$, GND = AGND = $V_{SSO} = 0V$
$T_{amb} = 0$ to 70^oC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLIES						
V_{CCO}	Output Supply Voltage		4.75	5	5.25	V
V_{DD}	Digital Supply Voltage		4.75	5	5.25	V
V_{CCA}	Analog Supply Voltage		4.75	5	5.25	V
DIGITAL OUTPUTS (I_0 = 1mA)						
V_{OL}	Low Level Output Voltage				0.4	V
V_{OH}	High Level Output Voltage		V_{CCO} - 0.4			V
I_{OZ}	Output Current in 3 State Mode		-20		20	µA
DIGITAL INPUTS (NTC, TCE)						
V_{IL}	Low Level Input Voltage		0	-0.4		V
V_{IH}	High Level Input Voltage		2		V_{DD}	V
I_{IL}	Low Level Input Current		-20		20	µA
I_{IH}	High Level Input Current		-20		20	µA
CLOCK INPUTS (CKIN, NCKIN)						
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{IH}	High Level Input Voltage		2		V_{CCA}	V
I_{IL}	Low Level Input Current		-500			µA
I_{IH}	High Level Input Current				500	µA
Z_I	Input Impedance (f_{IN} = 10MHz)		3			kΩ
C_I	Input Capacitance (f_{IN} = 10MHz)			6		pF
V_{CKIN} (pp)	Peak to Peak Differencial Cloch Input Voltage (1.6V DC Bias)		0.5		2	V
V_{IN} ANALOG VOLTAGE REFERENCED TO AGND						
VVIN(B)	Input Voltage (Bottom)			2.1		V
VVIN(0)	Input Voltage (Output Code = 0)			2.26		V
VVIN(T)	Input Voltage (Top)			3.7		V
VVIN(255)	Input Voltage (Output Code = 255)			3.54		V
VVIN(pp)	Input Voltage (Peak to Peak Value)		1.2	1.28	1.35	V
I_{IL}	Low Level Input Current (VVIN = 2.1V)			10		µA
I_{IH}	High Level Input Current (VVIN = 3.7V)		50	150	200	µA
REFERENCE RESISTANCE						
R_{REF}	Reference Resistance			200		Ω
ANALOG SIGNAL PROCESSING (f_{clk} = 30MHz)						
ILE	DC Integral Linearity Error				±1	LSB
DLE	DC Differential Linearity Error				±0.5	LSB
AILE	AC Integral Error (f_{IN} = 4.4MHz)				±2	LSB
Eff	Effective Bits (f_{IN} = 4.4MHz)			7.1		Bits
BW	-0.6dB Analog Bandwidth			14		MHz

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ELECTRICAL CHARACTERISTICS (Continued)

$V_{DD} = V_{CCA} = V_{CCO} = 4.75$ to 5.25V, GND = AGND = V_{SSO} = 0V

T_{amb} = 0 to 70°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TIMING (Figures 1 and 2)						
t_{ds}	Sampling Delay				2	ns
t_{HD}	Output Hold Time		5			ns
t_{do}	Output Delay Time				20	ns
t_{dz}	3 State Output Delay Time				25	ns

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Figure 1 : Timing Diagram

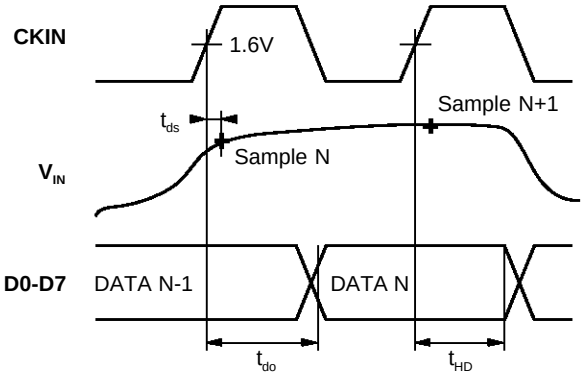

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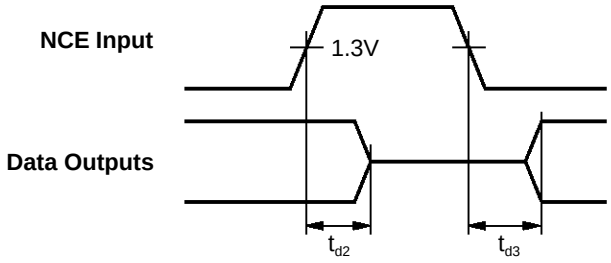
Figure 2 : 3 State Delay Timing Diagram



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The circuit has two clock inputs CKIN and NCKIN. There are four modes of operation.

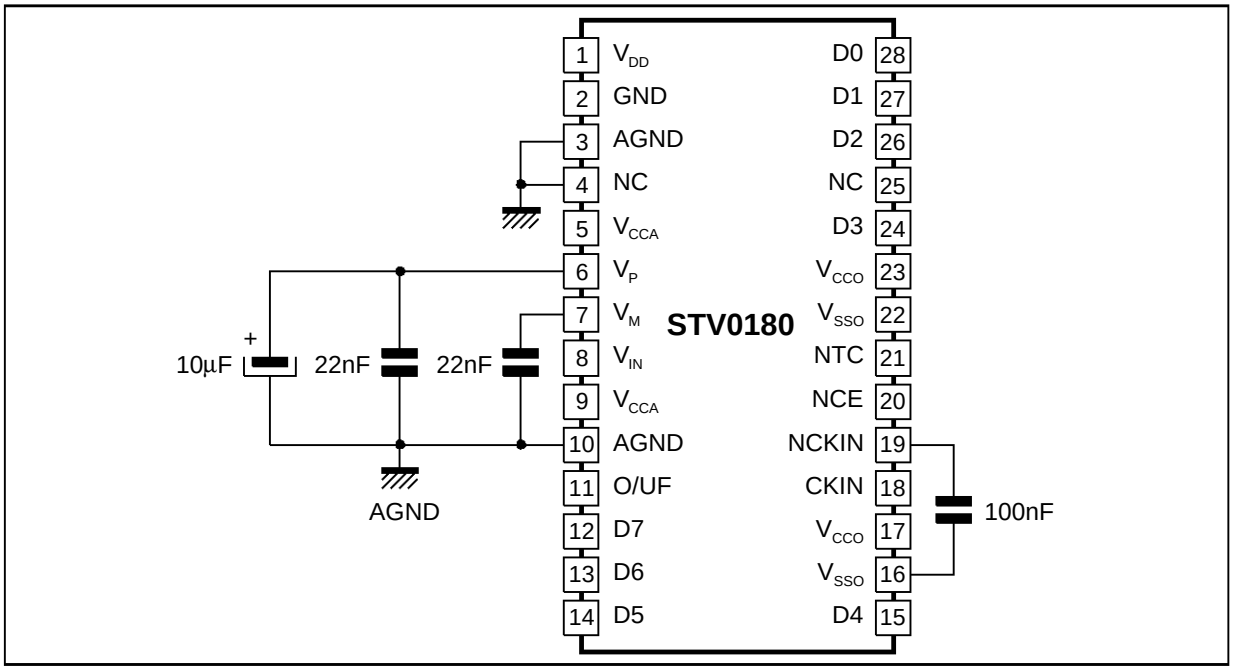
TTL ; NCKIN decoupled to V_{SSO} by a capacitor. CLK input is TTL threshold voltage of 1.6V and sampling on the LOW to HIGH transition of the input clock signal.

TTL ; CKIN decoupled to V_{SSO} by a capacitor. NCKIN input is TTL threshold voltage of 1.6V and sampling on a HIGH to LOW transistor.

AC drive mode ; When driving CKIN (NCKIN) input directly and with an AC signal of 0.5V (peak to peak value) imposed on a DC value of 1.6V sampling takes place on the LOW to HIGH (HIGH to LOW) transition of the clock signal.

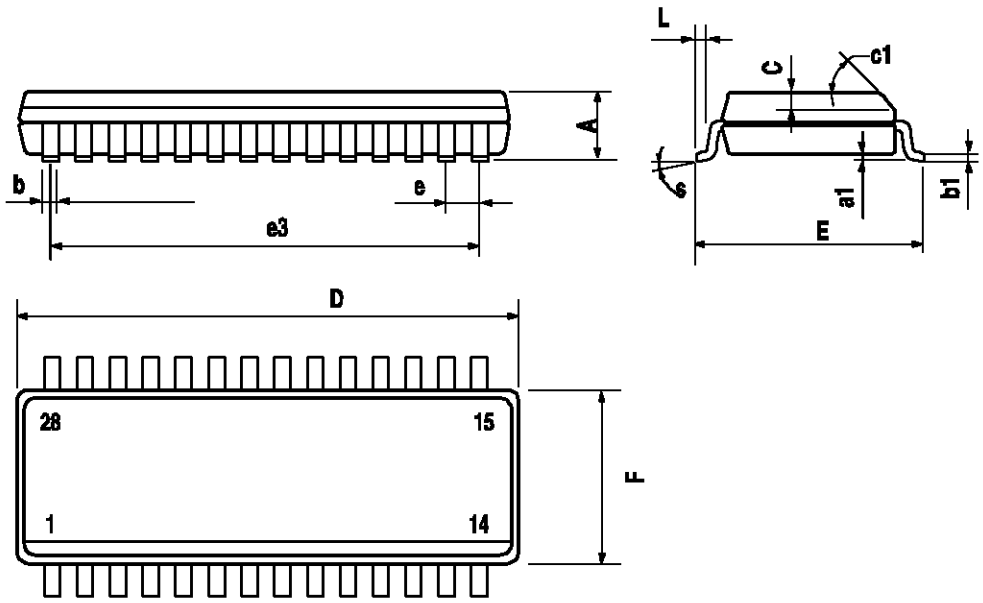
If one of the clock inputs is not driven, it is recommanded to decouple this input to V_{SSO} with a 100nF capacitor.

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE (SO)



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Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45^o (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8^o (max.)					

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